

Docket No.: 67161-098

AF / DW
PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In Application of

Takao KAMOSHIMA, et al.

Application No.: 10/657,094

Filed: September 09, 2003

For: INTERCONNECTION STRUCTURE

: Customer Number: 20277
:
: Confirmation Number: 9847
:
: Tech Center Art Unit: 2814
:
: Examiner: Nguyen, Dilinh P.
:

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief in support of the Notice of Appeal filed December 28, 2004. Please charge the Appeal Brief fee of \$500.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. 1.17 and 41.20, and in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 AJS:bt1:ntb
Facsimile: 202.756.8087
Date: February 15, 2005

**Please recognize our Customer No. 20277
as our correspondence address.**

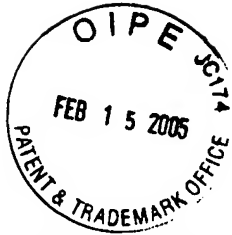


TABLE OF CONTENTS

I.	REAL PARTY IN INTEREST	1
II.	RELATED APPEALS AND INTERFERENCES	1
III.	STATUS OF CLAIMS	1
IV.	STATUS OF AMENDMENTS	2
V.	SUMMARY OF THE INVENTION	2
VI.	ISSUE	3
VII.	GROUPING OF CLAIMS	4
VIII.	ARGUMENT	4
IX.	PRAYER FOR RELIEF.....	13
	CLAIMS APPENDIX (APPEALED CLAIMS 1 THROUGH 9)	15



Docket No.: 67161-098

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of	:	Customer Number: 20277
	:	
Takao KAMOSHIMA, et al.	:	Confirmation Number: 9847
	:	
Application No.: 10/657,094	:	Tech Center Art Unit: 2814
	:	
Filed: September 09, 2003	:	Examiner: Nguyen, Dilinh P.
	:	
For: INTERCONNECTION STRUCTURE	:	

APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed December 28, 2004,
wherein Appellants appealed from the Primary Examiner's final rejection of claims 1 and 5 through 9.

I. REAL PARTY IN INTEREST

The Real Party in Interest is Renesas Technology Corp.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related Appeal or Interference.

02/17/2005 TTRAN1 00000027 500417 10657094
01 FC:1402 500.00 DA

III. STATUS OF CLAIMS

Claims 1 through 11 are pending in this Application, of which claims 2 through 4 have been allowed and claims 10 and 11 subject to objection, were indicated allowable if rewritten in independent form. Claims 1 and 5 through 9 have been finally rejected. It is from the final rejection of claims 1 and 5 through 9 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the issuance of the Final Office Action dated September 9, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention defined in independent claim 1 is directed to an interconnection structure for a semiconductor device, which is schematically illustrated in Fig. 1 and comprises a first conductive layer of copper 3; an insulating layer 4 formed thereon and having an opening comprising a hole 4a communicating with a groove 4b; a second conductive copper layer 6 filling the hole and groove; and a single barrier metal layer 5 lining the entire surface defining the hole and groove in insulating layer 4. Claim 1 specifies that the barrier metal layer has an opening at the bottom of the hole and that the second conductive layer 6 comes into direct contact with the first conductive layer 3 through that opening.

Independent claim 5 is also directed to an interconnection structure for a semiconductor device which is schematically illustrated in Fig. 16 and comprises a first copper layer 3 with an insulating layer 4 thereon. The insulating layer 4 has a first hole 4a, 4b and a second hole 4c reaching first conductive layer 3. A second conductive layer 6 is formed in the first hole 4a, 4b, but the second hole

4c is used as a dummy hole in that it does not (when filled with conductive material) electrically connect the first conductive layer 3 to another element.

The inventions defined in independent claims 1 and 5 address the microvoiding problems stemming from thermal stresses concentrated under a via when plating a copper film (page 2 of the written description of the specification, lines 4 through 8). Where an interconnection under a via has a large width, a defect occurs which increases via resistance or causes disconnection (page 2 of the written description, lines 8 through 13). The present invention addresses and solves such a problem by suppressing the concentration of voids in an interconnection under a via due to stress migration (page 2 of the written description, lines 15 through 18).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- 1. Claims 5 through 9 stand finally rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Moslehi; and**
- 2. Claim 1 stands finally rejected under 35 U.S.C. § 103 for obviousness predicated upon Li et al. in view of Kasai.**

VII. ARGUMENT

For the convenience of The Honorable Board of Patent Appeals and Interferences (the Board), Appellants separately argue the patentability of independent claim 1 and separately argue the patentability of independent claim 5. The patentability of claims 6 through 9 stands or falls with the patentability of independent claim 5.

1. **The rejection of claims 5 through 9 under 35 U.S.C. § 102 for lack of novelty as evidenced by Moslehi.**

The Examiner's Position.

The Examiner's rejection is predicated upon inaccurate factual determinations as to the teachings of Moslehi. Specifically, during prosecution Appellants argued that Moslehi does not disclose an interconnection structure corresponding to that defined in independent claim 5, which comprises a second hole, reaching the first conductive layer, and employed as a dummy hole which does not electrically connect the first conductive layer to another element. The Examiner's response is expressed at page 5 of the September 9, 2004 Final Office Action. In that exposition of the rejection, which crystallizes the pivotal issue to be resolved on Appeal, the Examiner referred again to Fig. 3 of Moslehi and asserted that the plug in the second hole on the right side is employed as a dummy hole. But saying so cannot make it so, and the Examiner conspicuously ducked pointing to any factual basis to support that assertion.

In addition, the Examiner inappropriately resorted to obviousness language in support of the rejection under 35 U.S.C. §103, concluding that one having ordinary skill in the art would have found it obvious to employ the second hole for a dummy hole as mechanical support which does not electrically connect the first conductive layer to another element (third full paragraph on page 6 of the September 9, 2004 Final Office Action).

Appellants' Position.

In rejecting a claim under 35 U.S.C. § 102 for lack of novelty the Examiner is required to identify wherein an applied reference is perceived to identically disclose each and every feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir.

1984). In relying upon the doctrine of inherency, the Examiner must provide a factual basis upon which to predicate the determination that an allegedly inherent feature is necessarily present within the applied prior art. *Crown Operations International Ltd. v. Solutia Inc.*, 289 F.3d 1367, 62 USPQ2d 1917 (Fed. Cir. 2002); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 34 USPQ2d 1565 *In re: Rijckaert supra*, *Continental Can Co. USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 20 USPQ2d 1746 (Fed. Cir. 1991). Neither of these burdens has been discharged. Moreover, the Examiner's factual statements are inaccurate and the Examiner's obviousness conclusion does not withstand scrutiny.

The plugs illustrated in Fig. 3 of Moslehi connect metal lines between two adjacent interconnect levels.

The Examiner committed clear factual error in asserting that the via plug on the right hand side of Moslehi's Fig. 3 device is used as a dummy hole. That this statement by the Examiner is clearly factually inaccurate is underscored by Moslehi in column 5, the paragraph commencing at line 49, wherein Moslehi states that both plugs 30 and 32 connect metal lines between two adjacent interconnect levels. Neither plug 30 nor plug 32 is a dummy plug. The only difference between the left hand side via plug 30 and the right hand side via plug 32 is that there is no barrier layer in via 32. Clearly, the Examiner's assertion that the plug on the right hand side (32) of Moslehi's Fig. 3 device is a dummy plug is factually inaccurate.

The Examiner's Obviousness Assertion.

The Examiner's obviousness conclusion has no place in the rejection under 35 U.S.C. § 102. At any rate, in the interests of the judicial economy, Appellants would point out that Moslehi merely

discloses that a plurality of dummy contacts and via plugs may be employed to provide additional mechanical support **if desired**. This evulgation appears in column 14 of Moslehi, (lines 8 through 12).

Clearly, Moslehi state that the use of dummy plugs "... is optional but not necessary." However, **if** this option is implemented, it is provided **between top and bottom etch-resistant layers**. But in Moslehi's Fig. 3 structure relied upon by the Examiner as a basis for denying patentability to the claimed invention, the second hole on the right hand side which the Examiner proposes to employ as a dummy, is **not between etch-resistant layers**. Rather, the second hole on the right hand side in the Fig. 3 embodiment of Moslehi **penetrates** an etch-resistant layer and reaches a lower conductive level Metal-1. Therefore, there is no factual technological basis to support the Examiner's conclusion that one having ordinary skill in the art would have been realistically motivated to employ the right hand side via 32 in Moslehi's Fig. 3 device as a dummy plug because it is not **between** two etch-resistant layers.

It is of interest to note that Moslehi's Fig. 3 embodiment does not even appear to represent Moslehi's invention, which is first exemplified in Fig. 6. Accordingly, the Examiner's attempt to read into Fig. 3 an optional embodiment of Moslehi's invention, which does not involve Fig. 3, is clearly inappropriate.

Further, as previously pointed out, if Moslehi's optional dummy support feature is implemented, it is provided **between etch-resistant layers**, not in contact with a lower conductive layer, as specifically required by claim 5. In this sense, Moslehi teaches away from the claimed invention.

Summary

Moslehi's failure to disclose an interconnection structure comprising features which identically correspond to those of independent claim 5, notably the second hole employed as a dummy hole, undermines the factual determination that Moslehi discloses an interconnection structure identically corresponding to that claimed. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Further, there is no apparent factual basis upon which to predicate the conclusion that one having ordinary skill in the art would somehow have been realistically impelled to modify Moslehi's Fig. 3 device to arrive at the claimed invention. *Teleflex Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 63 USPQ2d 1374, 1387 (Fed. Cir. 2002); *In re Lee*, 237 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).

Appellants, therefore submit that the Examiner's rejection of claims 5 through 9 under 35 U.S.C. § 102 for lack of novelty as evidenced by Moslehi is not factually viable. In addition, to whatever extent the Examiner's rejection is interpreted as a rejection under 35 U.S.C. § 103, Appellants submit the Examiner failed to establish a *prima facie* basis to deny patentability to claims 5 through 9 under 35 U.S.C. § 103 for obviousness predicated upon Moslehi.

2. The rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Li et al. in view of Kasai.

The Examiner's Position.

In rejecting claim 1 the Examiner **admitted** that Li et al. fail to disclose the use of a single barrier metal layer which is formed on the entire surface defining the hole and the groove in the insulating layer. The Examiner conspicuously avoided mentioning that Li et al. **require** forming two different barrier layers. At any rate, in order to make up for the admitted shortcoming of Li et al., the

Examiner turned to Kasai and concluded that one having ordinary skill in the art would have been motivated to modify the interconnection structure of Li et al. by providing a single barrier layer forming an entire surface defining a hole in a groove. The reason offered by the Examiner is the generalization that "... such single barrier layer would provide a method of manufacturing the device with a reduced number of steps ..." (ultimate sentence on page 4 of the September 9, 2004 Final Office Action).

Appellants Position.

1. There is no motivation.

The Examiner's generalization falls far short of making the requisite clear and particular factual findings as to a specific understanding or specific technological principle which would have realistically impelled one having ordinary skill in the art to modify the particular interconnection structure disclosed by Li et al. to arrive at the claimed invention, as judicially required. *Ecolochem Inc. v. Southern California Edison, Co.* 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); *In re Kotzab*, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). Specifically, and advertent to Fig. 6, Li et al. **do form a single barrier layer lining the entire opening**, i.e., barrier layer 92. So the Examiner does not have to go to Kasai and grope for a reason to modify the device of Li et al. by providing a single barrier layer.

What the Examiner fails to mention is that although Li et al. do deposit a single barrier layer to line the entire opening, Li et al. then conduct an etching step, which is illustrated in Fig. 7, to **remove** portions of the barrier layer 92. By removing portions of barrier layer 92, Li et al. **purposely** expose the top surfaces of the passivation layer 72 as well as cap layer 88. What the Examiner also fails to

mention is that this manipulative step of Li et al. of removing portions of barrier layer 92 to expose top surfaces of passivation layer 72 and cap layer 88 is considered by Li et al. as "... another important feature of the present invention ..." (column 5, lines 3 and 4).

It is, therefore, clear that a significant feature of the invention disclosed by Li et al. is removing portions of this single barrier layer so that it does **not** satisfy the requirement of independent claim 1 for a single barrier metal layer to be formed on an entire surface defining the hole and groove in the insulating layer. Clearly, Li et al. **teach away** from the claimed invention.

The Examiner's attempt to reconstruct the invention of Li et al. by doing what Li et al. do **not** want to do, i.e., form a single barrier layer to line the entire opening, is without any factual basis. Indeed, one having ordinary skill in the art cannot be said to have been realistically motivated to modify an applied reference in a manner inconsistent with the disclosed objective. *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992); *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); *In re Schulpen*, 390 F.2d 1009, 157 USPQ 52 (CCPA 1968).

2. The combined disclosures of the applied references do not yield a claimed invention.

Appellants do not agree that one having ordinary skill in the art would have been motivated to modify the interconnect structure disclosed by Li et al. by providing a single barrier metal layer lining the opening in view of Kasai for reasons previously argued. However, **if** this combination proposed by the Examiner were implemented, the claimed invention would **not** result. This is because claim 1 requires the barrier layer to have an opening in the bottom portion of the hole and that the second conductive layer comes into direct contact with the first conductive layer. If the device disclosed by Li et al. is modified in accordance with the teachings of Kasai, there would be **no** opening in the bottom barrier layer enabling direct connection between the first and second conductive layers, noting barrier

film 41 of Kasai. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

3. Evidence of Nonobviousness

As previously argued, Li et al. considered it important to remove portions of the barrier layer 92, thereby exposing the top surfaces of passivation layer 72 and cap layer 88 (Figs. 6 and 7). On the other hand, the claimed interconnection structure comprises a single barrier metal layer on the entire surface defining the opening. Thus, Li et al. clearly **teach away** from the claimed invention. This clear teaching away from the claimed invention constitutes evidence of **nonobviousness**. *Ecolochem Inc. v. Southern California Edison, Co.*, *supra*; *In re Bell*, 991 F.2d 781, 26 USPQ2d 1529 (Fed. Cir. 1993); *Specialty Composites v. Cabot Corp.*, 845 F.2d 981, 6 USPQ2d 1601 (Fed. Cir. 1988); *In re Marshall*, 578 F.2d 301, 198 USPQ 344 (CCPA 1978).

Summary

Based upon the foregoing Appellants submit that the Examiner failed to established a *prima facie* basis to deny patentability to the invention defined in independent claim 1 under 35 U.S.C. § 103. Moreover, upon giving due consideration to the clear teaching away from the claimed invention by the primary reference to Li et al., the conclusion appears inescapable that one having ordinary skill in the art would not have found the claimed subject matter as a whole obvious within the meaning of 35 U.S.C. § 103.

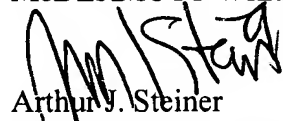
VIII. PRAYER FOR RELIEF

Based upon the arguments presented *supra*, Appellants submit that the imposed rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103 are not factually or legally viable. Appellants, therefore, solicit The Honorable Board to reverse the Examiner's rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 AJS:bjs:ntb
Facsimile: 202.756.8087
Date: February 15, 2005

**Please recognize our Customer No. 20277
as our correspondence address.**

CLAIMS APPENDIX

1. An interconnection structure, comprising:

a first conductive layer formed on a substrate and composed of a copper layer;

an insulating layer formed on said first conductive layer and having a hole reaching said first conductive layer and a groove communicating with said hole;

a second conductive layer formed within said insulating layer and composed of a copper layer electrically connected to said first conductive layer through said hole; and

a single barrier metal layer formed on an entire surface defining said hole and said groove in said insulating layer and formed between said second conductive layer and said hole, and said insulating layer; wherein

said barrier metal layer has an opening in a bottom portion of said hole, and said second conductive layer comes in direct contact with said first conductive layer through said opening.

5. An interconnection structure, comprising:

a first conductive layer formed on a substrate and composed of a copper layer;

an insulating layer formed on said first conductive layer and having a first hole and a second hole reaching said first conductive layer; and

a second conductive layer for electrical connection to another element, electrically connected to said first conductive layer through said first hole and formed within said insulating layer; wherein

said second hole is used as a dummy hole which does not electrically connect said first conductive layer to another element.

6. The interconnection structure according to claim 5, further comprising a dummy interconnection layer which is electrically connected to said first conductive layer through said second hole and does not electrically connect said first conductive layer to another element.

7. The interconnection structure according to claim 5, further comprising a third conductive layer filling said second hole, wherein
said third conductive layer is not electrically connected to other interconnection layer other than said first conductive layer.

8. The interconnection structure according to claim 5, wherein
said first conductive layer has a first interconnection portion with a large line width, and said second conductive layer has a second interconnection portion with a small line width, and
said first interconnection portion with the large line width is connected to said second interconnection portion with the small line width through said hole.

9. The interconnection structure according to claim 5, wherein
said first conductive layer has a first interconnection portion with a large line width, and a second interconnection portion with a small line width,
said second conductive layer has a third interconnection portion with a small line width, and
said second interconnection portion with the small line width is connected to said third interconnection portion with the small line width through said hole.